REMARKS

The Office Action mailed December 8, 2005 has been carefully considered. Reconsideration in view of the following remarks is respectfully requested.

Rejection(s) Under 35 U.S.C. § 103(a)

Claims 36-37, 39-40, 44-49 and 51-52 were rejected under 35 U.S.C. § 103(a) as unpatentable over Bergemont (U.S. pat. no. 6,563,731; hereinafter, "Bergemont") in view of Yamashita et al. (U.S. pat. no. 6,777,758; hereinafter, "Yamashita").

Claim 36 recites, *inter alia*, "a third p+ doped region and a fourth p+ doped region disposed in said second n- well, said third p+ doped region and said fourth p+ doped region together forming a tunneling junction." This feature is not disclosed or suggested in Bergemont. The Office Action points to Yamashita to remedy this shortcoming, along with the acknowledged failure of Bergemont to teach or suggest a well contact terminal coupled to a second n-well. The combination of Bergemont and Yamashita is proper, according to the Office Action, in order "to reduce the layout area of elements for fixing the potential of wells in a semiconductor device." Reducing layout area is always a desired goal. However, combining the teachings of Bergemont and Yamashita cannot be justified on these or other grounds for many reasons. Bergemont is directed to EEPROM memories. These operate on electron tunneling principals, primarily through gate oxides, and the conditions required to permit tunneling are very specific and impose strict limitations on operational, material and dimensional parameters. In addition, the object of

Bergemont is realize a device that can be fabricated consistent with CMOS processing procedures. Otherwise EEPROM devices can only be economically produced in bulk, and cannot be efficiently incorporated into SOC (system-on-chip) devices as Bergemont seeks to do. Yamashita, by comparison is not concerned with CMOS processing and introduces numerous fabrication steps that are inconsistent with CMOS processing and would add tremendous costs to the fabrication, in direct contravention of the stated goals of Bergemont. Therefore the teachings of these references are not properly combinable and in any case the presently claimed invention would not result because of the exacting operational constraints imposed by the physics of EEPROM devices.

According to the Manual of Patent Examining Procedure (M.P.E.P.),

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in the applicant's disclosure.[1]

In the present case, all three of these criteria are missing. Therefore the obviousness rejection of claims 36-40 and 44-52 based on the combination of Bergemont and Yamashita is improper and should be withdrawn.

[1] M.P.E.P § 2143.

Conclusion

In view of the preceding discussion, applicant respectfully urges that the claims of the present application define patentable subject matter and should be passed to allowance.

If the Examiner believes that a telephone call would help advance prosecution of the present invention, the Examiner is kindly invited to call the undersigned attorney at the number below.

Please charge any additional required fees, including fees for any extensions of time necessary to render timely the filing of the instant Amendment and/or Reply to Office Action, for which applicant hereby respectfully petitions, or credit any overpayment not otherwise credited, to our deposit account no. 50-1698.

Respectfully submitted,
THELEN REID & PRIEST, L.L.P.

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Khaled Shami
Reg. No. 38,745

Thelen Reid & Priest LLP
P.O. Box 640640
San Jose, CA 95164-0640
Tel. (408) 282-1855
Fax. (408) 287-8040